REMARKS

Claims 1-17 are pending in this application, of which claims 8-10 have been amended.

Claims 11-17 have been withdrawn from consideration. No new claims have been added.

Claims 1-7 stand rejected under 35 U.S.C. § 103(a) rejection of as unpatentable over **APA** in view of **Adachi et al.** (both previously applied).

Applicants respectfully traverse this rejection.

As noted in Applicants' response of February 22, 2006, the Examiner urges APA teaches that the superconductor or Josephson junction of the single flux quantum circuit requires small hysteresis in the current-voltage characteristic and the superconductor or Josephson junction of the interface circuit requires large hysteresis in the current-voltage characteristic, but fails to teach obtaining the desired current-voltage characteristics or hysteresis of the superconductor or Josephson junction of the single flux quantum circuit and the superconductor or Josephson junction of the interface circuit by changing materials of the junctions or using different materials for the junctions.

The Examiner has cited <u>Adachi et al.</u> for teaching that the desired current-voltage characteristics or hysteresis of superconductor or Josephson junctions can be obtained by using different material for the junctions. See [0048] to [0060].

Applicants respectfully disagree with the Examiner's characterization of what <u>APA</u> teaches. Page 2, line 16 to page 3, line 9 disclose that, in <u>APA</u>, the operation of the SFQ circuit and the operation of the interface circuit are both carried out in a small operational region which compromises performance for both circuits. This passage discloses only that the ideal relation

between the critical current density and the operational region is <u>different</u> for each of the SFQ circuit and the interface circuit. This does not suggest that <u>APA</u> teaches separate Josephson junctions for each of the SFQ circuit and the interface circuit, where the Josephson junctions have different voltage characteristics.

Paragraph [0006] of <u>Adachi et al.</u> teaches the ramp edge junctions recited in claims 5-7, but, like <u>APA</u>, fails to teach, mention or suggest using separate Josephson junctions for each of the SFQ and the interface circuit, as recited in claim 1 of the instant application.

<u>APA</u> discloses that a latch driver circuit, thought to be <u>unsuitable for the formation of a high temperature superconductor</u>, is used for the interface circuit, and requires hysteresis, while the high temperature superconductor junction used for the SFQ circuit requires a "sufficiently small" hysteresis. Thus, <u>APA</u> fails to teach, mention or suggest the use of a "second Josephson junction" for the interface circuit, as claimed in the present invention.

In other words, the present invention uses the high temperature superconductor Josephson junction, which is generally though to be unsuitable for the latch driver circuit (interface circuit) since the hysteresis is small and the operation region is extremely limited, as in <u>APA</u>.

Thus, the 35 U.S.C. § 103(a) rejection should be withdrawn.

The Examiner has indicated that claims 8-10 would be allowable if rewritten in independent form. Accordingly, claims 8-10 have been amended to be rewritten in independent form.

In view of the aforementioned amendments and accompanying remarks, claims 1-10, as amended, are in condition for allowance, which action, at an early date, is requested.

U.S. Patent Application Serial No. 10/809,919 Response to Office Action dated May 2, 2006

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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PATENT TRADEMARK OFFICE

Enclosures:

Petition for Extension of Time

Amendment Transmittal

Check in the amount of \$650.00

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